



STAMFORD COLLEGE
SCHOOL OF COMPUTER SCIENCES
DIPLOMA IN INFORMATION TECHNOLOGY

STC111 : COMPUTER ARCHITECTURE

Date : 16 May 2007 (Wednesday)
Time : 9.00 a.m. – 11.00 a.m.

Duration: 2 hours

Instructions to Candidates

Answer ALL questions.

Please ensure that this examination paper contains FOUR questions on TWO printed pages before you start the examination.

Books, papers and other written materials are not allowed to be brought into the examination hall. A candidate who violates the examination rules of Stamford College or commits a malpractice will be disqualified from the examination.

Candidates may use calculators provided the calculators give no printout, have no work display facilities, are silent and cordless.

Write your Examination Index Number on each page of your answer booklet.

Answer ALL questions**Question 1**

- (a) Simplify the following expressions in (i) Sum of Products and Product of sums form. Draw a logic circuit for Sum of product using NAND gates only.

$$F = AC' + B'D + A'CD + ABCD.$$

(13 marks)

- (b) Determine by means of the truth table by validity of De-Morgan's theorem for 3 variables

$$(ABC)' = A' + B' + C'.$$

(8 marks)

- (c) Explain the difference between the combination circuit and sequential circuits.

(4 marks)

(Total = 25 marks)

Question 2

- (a) Explain the function of following registers.

- (i) PC
- (ii) MAR
- (iii) IR
- (iv) MDR
- (v) MBR
- (vi) ACC

(6 marks)

- (b) What are the functional groups into which the lines of a typical system bus are classified? Briefly describe their functions.

(9 marks)

- (c) Explain the following sequence of operations represent a typical fetch cycle. Illustrate these operations using a block diagram.

MAR ← (PC)
 MBR ← Memory
 PC ← (PC) + 1
 IR ← (MBR)

(10 marks)

(Total = 25 marks)

Question 3

- (a) The following assignment statement is given:

$$A = A * B + C * D * E$$

Show how you can implement the above statement using instructions for the following machines:

- (i) 0-Address machine
- (ii) 1-Address machine
- (iii) 2-Address machine

You should assume that variables (a,b,c,d and e) are associated with the memory location 100,104,108,112 and 116 respectively. In addition, you may assume that memory location 200 is available for temporary use

(11 marks)

- (b) Let the contents of an Associative memory be as follows:

W₀ 110010101

W₁ 101010101

W₂ 110011001

W₃ 100110001

Write value of the Match register (M) in the following cases.

K = 000011111 and A = 110010101

(5 marks)

- (c) Assume the computer Y has the main memory with the capacity 32K words of 12 bits each. The cache is capable of storing 512 of these words at any given time. Inside the cache, there are 64 blocks and 8 words each. Using the above information, specify the main memory using the following mapping techniques:

- (i) An Associative mapping.
- (ii) A direct mapping.
- (iii) 4-way associative mapping.
- (iv) The main memory address is 000010AF₁₆.

(9 marks)

(Total = 25 marks)

Question 4

- (a) List FOUR characteristics of Reduced Instruction Set of Computer. (4 marks)
 - (b) Briefly explain Programmed I/O. (6 marks)
 - (c) A memory has a capacity of 4 k X 8. How many data lines and address lines does it have? (4 marks)
 - (d) Illustrate the memory hierarchy and its components. (6 marks)
 - (e) Explain the concept of virtual memory. (5 marks)
- (Total = 25 marks)

- END OF PAPER -